TABLE 3-2 Move or Copy Instructions

Mnemonics	Operand	Description	Word	Cycle	Status bits affected
MOVLW	8-bit	Load 8-bit number into W register	1	1	
MOVWF	F, a	Copy W register into F (Data) register	1	1	
MOVFF	Fs, Fd	Copy source data register (Fs) into destination (Fd) data register	2	2	
MOVF	F, d, a	Copy F register into itself or W register	1	1	N Z
CLRF	F, a	Clear F (File/Data) register	1	1	Z
SETF	F, a	Set all bits to 1 in F (Data) register	1	1	
SWAPF	F, d, a	Exchange low-order four bits with high order four bits in File (Data) register	1	1	
LFSR	F, 12-bit	Load 12-bit address into File Select register	2	2	
PUSH		Copy address of next instruction on stack	1	1	
POP		Discard address on top of stack	1	1	

TABLE 3-3 Arithmetic Instructions

Mnemonics	Operand	Description	Word	Cycle	Status bits affected
ADDLW	8-bit	Add 8-bit number to W register	1	1	N OV Z DC C
ADDWF	F, d, a	Add WREG to File (Data) register and save result in W or F	1	1	N OV Z DC C
ADDWFC	F, d, a	Add WREG, File (Data) register, and Carry and save the result in W or F	1	1	N OV Z DC C
SUBLW	8-bit	Subtract WREG from 8-bit number	1	1	N OV Z DC C
SUBWF	F, d, a	Subtract WREG from File (Data) register and save result in W or F	1	1	N OV Z DC C
SUBWFB	F, d, a	Subtract WREG and Borrow from File (Data) register and save result in W or F	1	1	N OV Z DC C
SUBFWB	F, d, a	Subtract File (Data) register, Borrow, from WREG and save result in W or F	1	1	N OV Z DC C
INCF	F, d, a	Increment File (Data) register and save result in W or F	1	1	N OV Z DC C
DECF	F, d, a	Decrement File (Data) register and save result in W or F	1	1	N OV Z DC C
COMF	F, d, a	Complement File (Data) register and save result in W or F1	1	1	N Z
NEGF	F, a	Take 2's complement File (Data) register	1	1	N OV Z DC C
MULLW	8-bit	Multiply WREG and 8-bit and save result in PRODH:PRODL	1	1	

TABLE 3-7 Skip Instructions (Check Data Condition and Skip Next Instruction)

Mnemonics	Operand	Description	Word	Cycle	Status bits affected
BTFSC	F, b, a	Test bit b of register F where b = 0 to 7; skip the next instruction if bit = 0	1	1/2	
BTFSS	F, b, a	Test bit b of register F where b = 0 to 7; skip the next instruction if bit = 1	1	1/2	
CPFSEQ	F, a	Compare F with W register, skip if F = W	1	1/2	
CPFSGT	F, a	Compare F with W register, skip if F > W	1	1/2	
CPFSLT	F, a	Compare F with W register, skip if F < W	1	1/2	
TSTFSZ	F, a	Test F; skip if F = 0	1	1/2	
DECFSZ	F, d, a	Decrement F and save either in W or F; skip if result = 0	1	1/2	
DECFSNZ	F, d, a	Decrement F and save either in W or F; skip if result ≠ 0	1	1/2	
INCFSZ	F, d, a	Increment F and save either in W or F; skip if result = 0	1	1/2	
INCFSNZ	F, d, a	Increment F and save either in W or F; skip if result ≠ 0	1	1/2	

TABLE 3-8 Table Read and Write

Mnemonics	Operand	Description	Word	Cycle	Status bits affected
TBLRD*		Read Table from Program Memory pointed to TBLPTR into TABLAT	1	2	
TBLRD* +		Read Table from Program Memory pointed to TBLPTR into TABLAT and increment TBLPTR	1	2	
TBLRD* -		Read Table from Program Memory pointed to TBLPTR into TABLAT and decrement TBLPTR	1	2	
TBLRD +*		Increment TBLPTR and read Table from Program Memory pointed to TBLPTR into TABLAT	1	2	
TBLWT*		Write Table into Program Memory pointed to TBLPTR from TABLAT	1	2	
TBLWT*+		Write Table into Program Memory pointed to TBLPTR from TABLAT and increment TBLPTR	1	2	
TBLWT*-		Write Table into Program Memory pointed to TBLPTR from TABLAT and decrement TBLPTR	1	2	
TBLWT +*		Increment TBLPTR and write Table into Program Memory pointed to TBLPTR from TABLAT	1	2	

TABLE 3-9 Control Instructions

Mnemonics	Operand	Description	Word	Cycle	Status bits affected
CLRWDT		Clear Watchdog Timer	1	1	
RESET		Reset all registers and flags	1	1	N OV Z DC C
SLEEP		Go into standby mode	1	1	
NOP		No operation	1	1	

TABLE 3-4 Logic Instructions

Mnemonics	Operand	Description	Word	Cycle	Status bits affected
ANDLW	8-bit	Logically AND 8-bit number with WREG	1	1	N Z
ADDWF	F, d, a	Logically AND WREG with File (Data) register and save result in W or F	1	1	N Z
IORLW	8-bit	Logically OR 8-bit number with WREG	1	1	N Z
IORWF	F, d, a	Logically OR WREG with File (Data) register and save result in W or F	1	1	N Z
XORLW	8-bit	Exclusive OR 8-bit number with WREG	1	1	N Z
XORWF	F, d, a	Exclusive OR WREG with File (Data) register and save result in W or F	1	1	N Z

TABLE 3-5 Program Redirection (Branch and Call Instructions)

Mnemonics	Operand	Description	Word	Cycle	Status bits affected
BC	n	Branch if Carry = 1 within ± 64 Words	1	1/2	
BNC	n	Branch if Carry = 0 within ± 64 Words	1	1/2	
BZ	n	Branch if Z = 1 within ± 64 Words	1	1/2	
BNZ	n	Branch if Z = 0 within ± 64 Words	1	1/2	
BN	n	Branch if N = 1 within ± 64 Words	1	1/2	
BNN	n	Branch if N = 0 within ± 64 Words	1	1/2	
BOV	n	Branch if OV = 1 within ± 64 Words	1	1/2	
BNOV	n	Branch if OV = 0 within ± 64 Words	1	1/2	
BRA	nn	Branch unconditionally within ± 512 Words	1	2	
GOTO	Address	Go to 20-bit address unconditionally	2	2	
Call and Return Instructions					
RCALL	nn	Call subroutine within ± 512 words	1	2	
CALL	20-bit, s	Call subroutine. Save W, STATUS, & BSR in their shadow registers if s = 1	2	2	
RETURN,	s	Return from subroutine. Restore W, STATUS, & BSR from shadow registers if s = 1	1	2	
RETLW	8-bit	Return 8-bit number to W	1	2	
RETFIE	s	Return from interrupt and if s =1, W, STATUS, & BSR values are restored	1	2	

TABLE 3-6 Bit Manipulation (Bit Set, Reset, Toggle, and Rotate)

Mnemonics	Operand	Description	Word	Cycle	Status bits affected
BCF	F, b, a	Clear bit b of register F where b = 0 to 7	1	1	
BSF	F, b, a	Set bit b of register F where b = 0 to 7	1	1	
BTG	F, b, a	Toggle bit b of register F where b = 0 to 7	1	1	
RLCF	F, d, a	Rotate File (data) register Left through Carry and save result in F or W	1	1	N Z C
RLNCF	F, d, a	Rotate File (data) register Left excluding Carry and save result in F or W	1	1	N Z
RRCF	F, d, a	Rotate File (data) register Right through Carry and save result in F or W	1	1	N Z C
RRNCF	F, d, a	Rotate File (data) register Right excluding	1	1	N Z